

Brent Lee

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EDUCATION

BS: Electrical Engineering & Computer Science – 3.8 GPA

Expected May 2028

University of California, Berkeley

- Relevant Coursework: **Digital Design & Integrated Circuits**, ASIC Lab, Computer Architecture, Data Structures, Intro to Circuits/Devices, Mechanics and E&M, Signals & Systems
- Current Coursework: Digital Communications, MEMS, Microelectronic Circuits
- Plan to Take: Advanced Digital ICs and Systems, Fundamental Algorithms for EDA & Verification, Tapeout

WORK EXPERIENCE

Electromagnetic Effects Qualification Intern & Part-Time

May 2026 - Present

The Boeing Company – Boeing Commercial Airplanes – Airplane Systems

Everett, WA

- Built a Python app that leverages LLMs to **automate certification report generation** from ground test procedures, reducing report turnaround from **months to weeks** and improving consistency across engineering deliverables
- Traced component-level system boundaries, interactions, and net connections to support qualification analysis, and **evaluated supplier qualification packages** against hardware and software **compliance** requirements
- Executed compatibility transient pin injection testing for component-level qualification and supported aircraft ground tests by verifying installation data and preparing test procedures

Wireless and Navigation/Digital Communications Intern

May 2025 - August 2025

The Aerospace Corporation

El Segundo, CA

- Improved interference rejection by 40dB+ for a satellite received signal by assembling and testing an **RF front end** with mixers, IF filtering, and a spectrum analyzer to amplify the signal and **suppress out-of-band interferers**
- Built custom Software Defined Radio (SDR) protocol stack with **2FSK modulation**, designing packet framing with **preamble synchronization**, Forward Error Correction (FEC), and **CRC** validation for reliable data RF link
- Boosted transmitter block throughput by porting signal processing codebase from Python to **C++** with **Intel Performance Primitives** and restructuring frame construction to eliminate buffer underflow
- Built resilient **multi-link control network** in **Python** using ZeroMQ, heartbeat monitoring, and YAML-based configuration

INVOLVEMENT & PROJECTS

ASIC Lab Digital Design Project | Apple Design Project Finalist

March 2026 – May 2026

EECS 151: Digital Design & Integrated Circuits

- Designed and verified a **3-stage pipelined RV32I processor** in **SystemVerilog** with forwarding and parameterized direct-mapped/N-way set-associative cache with PLRU replacement built on sky130 SRAM macros
- Drove the full ASIC implementation flow in **Synopsys/Innovus via Hammer**, hand tuning SRAM macro placement to resolve DRC violations and verifying the routed netlist met timing and passed the full test suite
- Optimized for class **energy × area** figure of merit (FOM) by sweeping synthesis clock constraint, evaluating direct-mapped vs. set-associative **cache configurations**, and assessing **branch predictor** tradeoffs to achieve final 42 FOM

Electrical Team Project Lead

August 2025 - Present

Berkeley Solar Car (CalSol)

- Led a 3-person team designing a 4-layer microcontroller-based **battery management control PCB** in **KiCad** for CalSol's Gen XI solar car; completed schematic and layout, with bring-up and firmware integration next
- Implemented **ISO-SPI hardware interfaces** to battery module logic boards using transformer coupling, isolation-moat constraints, and differential routing
- Designed **power, control, and status circuitry** for contactor actuation and thermal management, including low-side drivers, fused fan power for multiple PWM cooling fans, an SPI display, and LED indicators

Avionics Deputy

August 2024 – May 2026

Space Technologies and Rocketry (STAR) at Berkeley

- Designing a payload power system around **LiFePO4** storage, **solar charging**, and **USB PD** input to support autonomous microcontroller-based **data collection for 24+ hours after rocket landing**
- Built fiberglass rocket targeting 2100ft apogee using **OpenRocket** simulations for sizing and performance
- Designed and assembled an **ESP32-S3** avionics board in Altium Designer for **in-flight sensing and telemetry**; programmed firmware for flash memory, barometer, and IMU in **C** using **Arduino IDE**

SKILLS

Programming Languages and Frameworks: SystemVerilog | Python | C | C++ | Java

EDA & Hardware: Altium Designer | KiCAD | Synopsys VCS/Design Compiler | Cadence Innovus | Hammer | Verilator | Verdi | Solidworks

Tools: Linux | Git | Spectrum Analyzer/Oscilloscope | Jupyter | Arduino IDE | SOLIDWORKS

Domains: Digital ASIC Design | PCB Design | Signal Processing/RF | Computer Vision | Cybersecurity